Lab 4 - M. D. B. Perera - 210465P

**Assigned Task:**

* Building a **D Flip-Flop**.
* Building the ‘slowed-down’ version of the internal clock of BASYS 3.
* Building a **3-bit Counter** using the Slowed-down clock & three D Flip-Flops.
* Testing the project on Basys 3.

**Table:**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Qn | | | **Button** | Qn+1 | | | **D2** | **D1** | **D0** |
| **Q2** | **Q1** | **Q0** | **Q2** | **Q1** | **Q0** |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |

**Karnaugh Map of D0:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q0Dir**  **Q2Q1** | **00** | **01** | **11** | **10** |
| **00** | 1 | 0 | 0 | 1 |
| **01** |  |  | 1 | 1 |
| **11** | 0 | 1 | 1 | 0 |
| **10** | 0 | 0 |  |  |

D0 = Q1Dir + 2

**Karnaugh Map of D1:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q0Dir**  **Q2Q1** | **00** | **01** | **11** | **10** |
| **00** | 0 | 0 | 0 | 1 |
| **01** |  |  | 0 | 1 |
| **11** | 0 | 1 | 1 | 1 |
| **10** | 0 | 1 |  |  |

D0 = Q2 + Q0

**Karnaugh Map of D2:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q0Dir**  **Q2Q1** | **00** | **01** | **11** | **10** |
| **00** | 0 | 1 | 0 | 0 |
| **01** |  |  | 0 | 1 |
| **11** | 1 | 1 | 0 | 1 |
| **10** | 0 | 1 |  |  |

D0 = 0 + Q1

**VHDL Files:**

1. D Flip-Flop Design Source File

----------------------------------------------------------------------------------

-- Company: University of Moratuwa

-- Engineer: Dulina Perera

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-- Create Date: 01.04.2023 09:00:16

-- Design Name: D Flip-Flop

-- Module Name: D\_FF - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity D\_FF is

port (

D, Res, Clk : in STD\_LOGIC;

Q : out STD\_LOGIC := '0';

Qbar : out STD\_LOGIC := '1'

);

end D\_FF;

architecture behavioral of D\_FF is begin

process (Clk) begin

if (rising\_edge(Clk)) then

if (Res = '1') then

Q <= '0';

Qbar <= '1';

else

Q <= D;

Qbar <= NOT D;

end if;

end if;

end process;

end behavioral;

1. D Flip-Flop Simulation Source File

----------------------------------------------------------------------------------

-- Company: University of Moratuwa

-- Engineer: Dulina Perera

--

-- Create Date: 01.04.2023 09:04:53

-- Design Name: D Flip-Flop(Simulation)

-- Module Name: D\_FF\_Sim - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

--

-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity D\_FF\_Sim is

-- port ( );

end D\_FF\_Sim;

architecture behavioral of D\_FF\_Sim is

component D\_FF

port (

D, Res, Clk : in STD\_LOGIC;

Q, Qbar : out STD\_LOGIC

);

end component;

signal D, Res, Clk : STD\_LOGIC; -- Initialize inputs

signal Q, Qbar: STD\_LOGIC;

begin

UUT: D\_FF port map(

D => D,

Res => Res,

Clk => Clk,

Q => Q,

Qbar => Qbar

);

-- Clock generator process

process begin

D <= '1';

Res <= '1';

Clk <= '0';

wait for 100ns;

Clk <= '1';

wait for 100ns;

Clk <= '0';

Res <= '0';

wait for 100ns;

Clk <= '1';

wait for 100ns;

Clk <= '0';

D <= '0';

Res <= '1';

wait for 100ns;

Clk <= '1';

wait for 100ns;

Clk <= '0';

Res <= '0';

wait for 100ns;

Clk <= '1';

wait;

end process;

end behavioral;

1. Slowed-down Clock Design Source File

----------------------------------------------------------------------------------

-- Company: University of Moratuwa

-- Engineer: Dulina Perera

--

-- Create Date: 08.04.2023 12:08:10

-- Design Name: Slowed-down Clock

-- Module Name: Slow\_Clk - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity Slow\_Clk is

port (

Clk\_in : in STD\_LOGIC;

Clk\_out : out STD\_LOGIC := '0'

);

end Slow\_Clk;

architecture Behavioral of Slow\_Clk is

signal Count : integer := 1;

signal Clk\_status : STD\_LOGIC := '0';

begin

-- Generate a 1 Hz clock from 100 MHz input clock.

process(Clk\_in) begin

-- Count the number of rising edges.

if (rising\_edge(Clk\_in)) then

Count <= Count + 1;

-- If 'Count' exceeds 50 million then invert 'Clk\_status'.

if (Count = 50000000) then

Clk\_out <= NOT Clk\_status;

Clk\_status <= NOT Clk\_status;

Count <= 1; -- reset counter

end if;

end if;

end process;

end Behavioral;

1. Slowed-down Clock Simulation Source File

----------------------------------------------------------------------------------

-- Company: University of Moratuwa

-- Engineer: Dulina Perera

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-- Create Date: 08.04.2023 12:23:56

-- Design Name: Slowed-down Clock(Simulation)

-- Module Name: Slow\_Clk\_Sim - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity Slow\_Clk\_Sim is

-- port ( );

end Slow\_Clk\_Sim;

architecture Behavioral of Slow\_Clk\_Sim is

component Slow\_Clk

port (

Clk\_in : in STD\_LOGIC;

Clk\_out : out STD\_LOGIC

);

end component;

signal Clk\_in: STD\_LOGIC;

signal Clk\_out : STD\_LOGIC;

begin

UUT: Slow\_Clk port map(

Clk\_in => Clk\_in,

Clk\_out => Clk\_out

);

process begin

for i in 0 to 49 loop

Clk\_in <= '1';

wait for 10 ns;

Clk\_in <= '0';

wait for 10 ns;

end loop;

wait;

end process;

end Behavioral;

1. Counter Design Source File

----------------------------------------------------------------------------------

-- Company: University of Moratuwa

-- Engineer: Dulina Perera

--

-- Create Date: 08.04.2023 14:32:29

-- Design Name: 3-bit Counter

-- Module Name: Counter - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity Counter is

port (

Dir, Res, Clk : in STD\_LOGIC;

Q : out STD\_LOGIC\_VECTOR(2 downto 0) := "000"

);

end Counter;

architecture Behavioral of Counter is

component D\_FF

port (

D : in STD\_LOGIC;

Res: in STD\_LOGIC;

Clk : in STD\_LOGIC;

Q : out STD\_LOGIC;

Qbar : out STD\_LOGIC

);

end component;

component Slow\_Clk

port (

Clk\_in : in STD\_LOGIC;

Clk\_out: out STD\_LOGIC

);

end component;

signal D0, D1, D2: STD\_LOGIC;

signal Q0, Q1, Q2 : STD\_LOGIC;

signal Clk\_slow : STD\_LOGIC;

begin

Slow\_Clk0 : Slow\_Clk

port map (

Clk\_in => Clk,

Clk\_out => Clk\_slow

);

D0 <= (Q1 AND Dir) OR ((NOT Q2) AND (NOT Dir));

D1 <= (Q2 AND Dir) OR (Q0 AND (NOT Dir));

D2 <= ((NOT Q0) AND Dir) OR (Q1 AND (NOT Dir));

D\_FF0 : D\_FF

port map (

D => D0,

Res => Res,

Clk => Clk\_slow,

Q => Q0,

Qbar => open

);

D\_FF1 : D\_FF

port map (

D => D1,

Res => Res,

Clk => Clk\_slow,

Q => Q1,

Qbar => open

);

D\_FF2 : D\_FF

port map (

D => D2,

Res => Res,

Clk => Clk\_slow,

Q => Q2,

Qbar => open

);

Q <= Q2 & Q1 & Q0; -- Concatenate 'Q2', 'Q1', 'Q0' to form 'Q'.

end Behavioral;

1. Counter Simulation Source File

----------------------------------------------------------------------------------

-- Company: University of Moratuwa

-- Engineer: Dulina Perera

--

-- Create Date: 08.04.2023 16:51:32

-- Design Name: Counter(Simulation)

-- Module Name: Counter\_Sim - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

--

-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity Counter\_Sim is

-- port ( );

end Counter\_Sim;

architecture Behavioral of Counter\_Sim is

component Counter

port (

Dir, Res, Clk : in STD\_LOGIC;

Q : out STD\_LOGIC\_VECTOR(2 downto 0)

);

end component;

signal Dir, Res, Clk : STD\_LOGIC;

signal Q : STD\_LOGIC\_VECTOR(2 downto 0);

begin

UUT: Counter port map(

Dir => Dir,

Res => Res,

Clk => Clk,

Q => Q

);

process begin

Res <= '0';

Dir <= '0';

for i in 0 to 5 loop

for i in 0 to 9 loop

Clk <= '1';

wait for 5 ns;

Clk <= '0';

wait for 5 ns;

end loop;

end loop;

Dir <= '1';

for i in 0 to 5 loop

for i in 0 to 9 loop

Clk <= '1';

wait for 5 ns;

Clk <= '0';

wait for 5 ns;

end loop;

end loop;

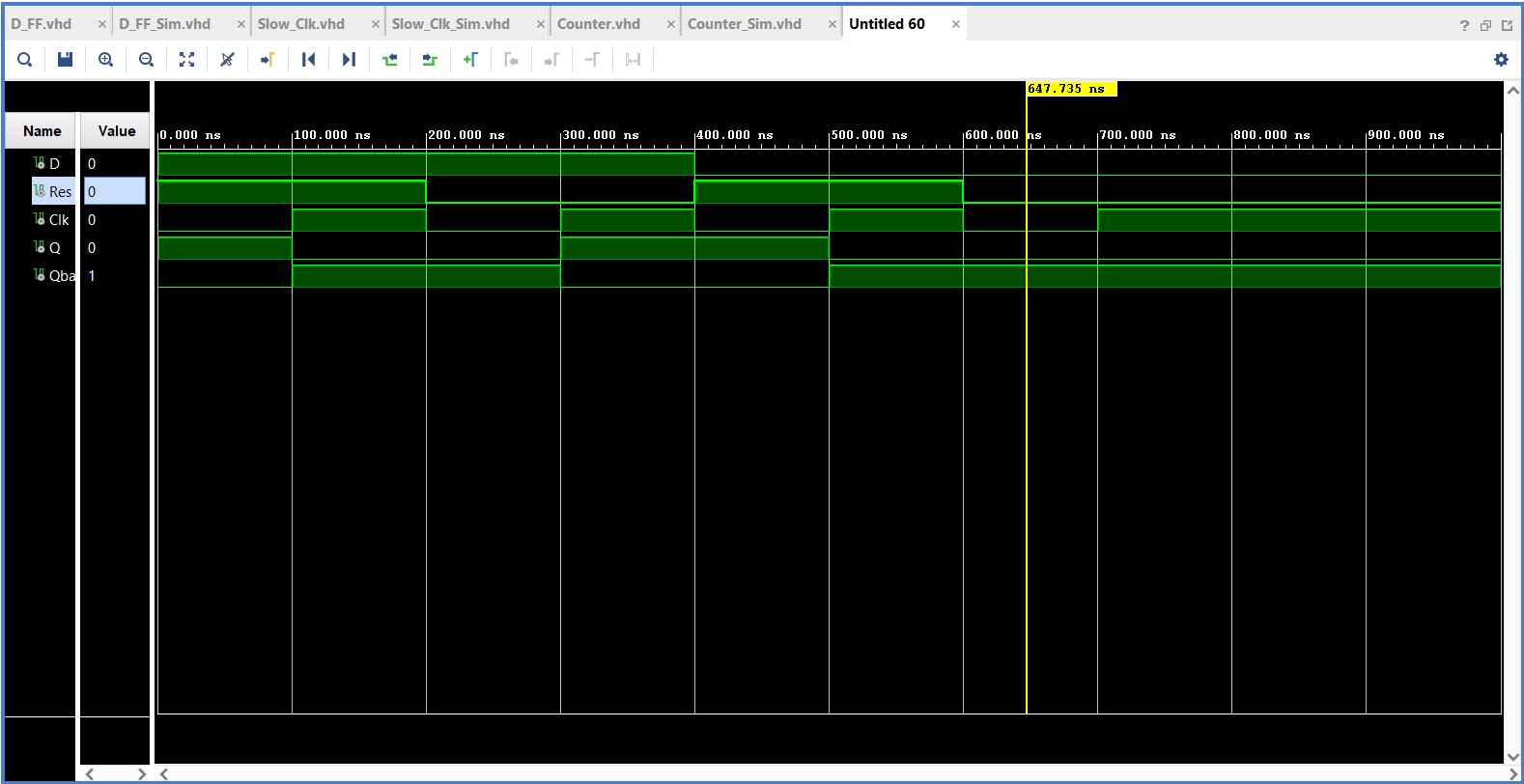
wait;

end process;

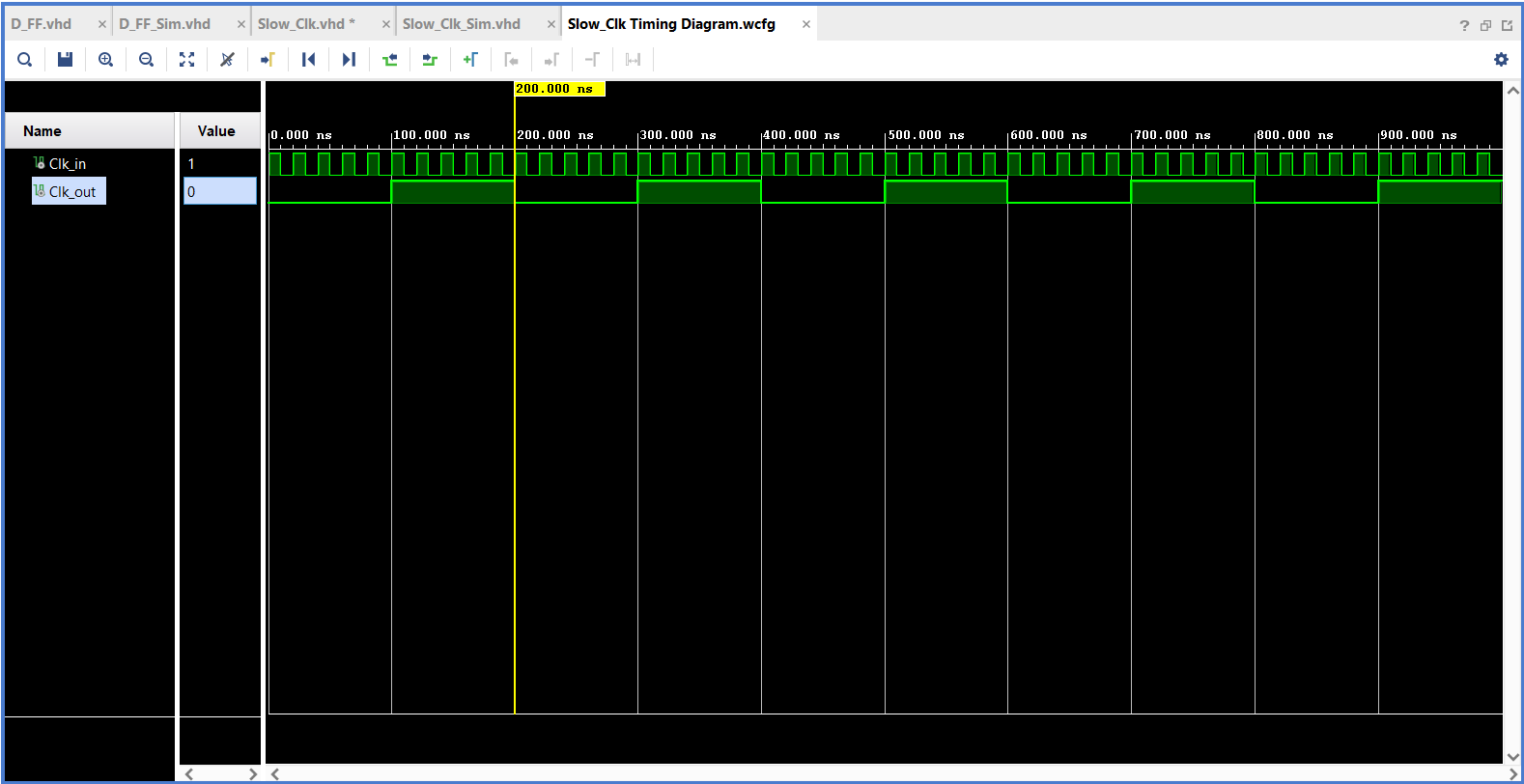
end Behavioral;

**Timing Diagrams:**

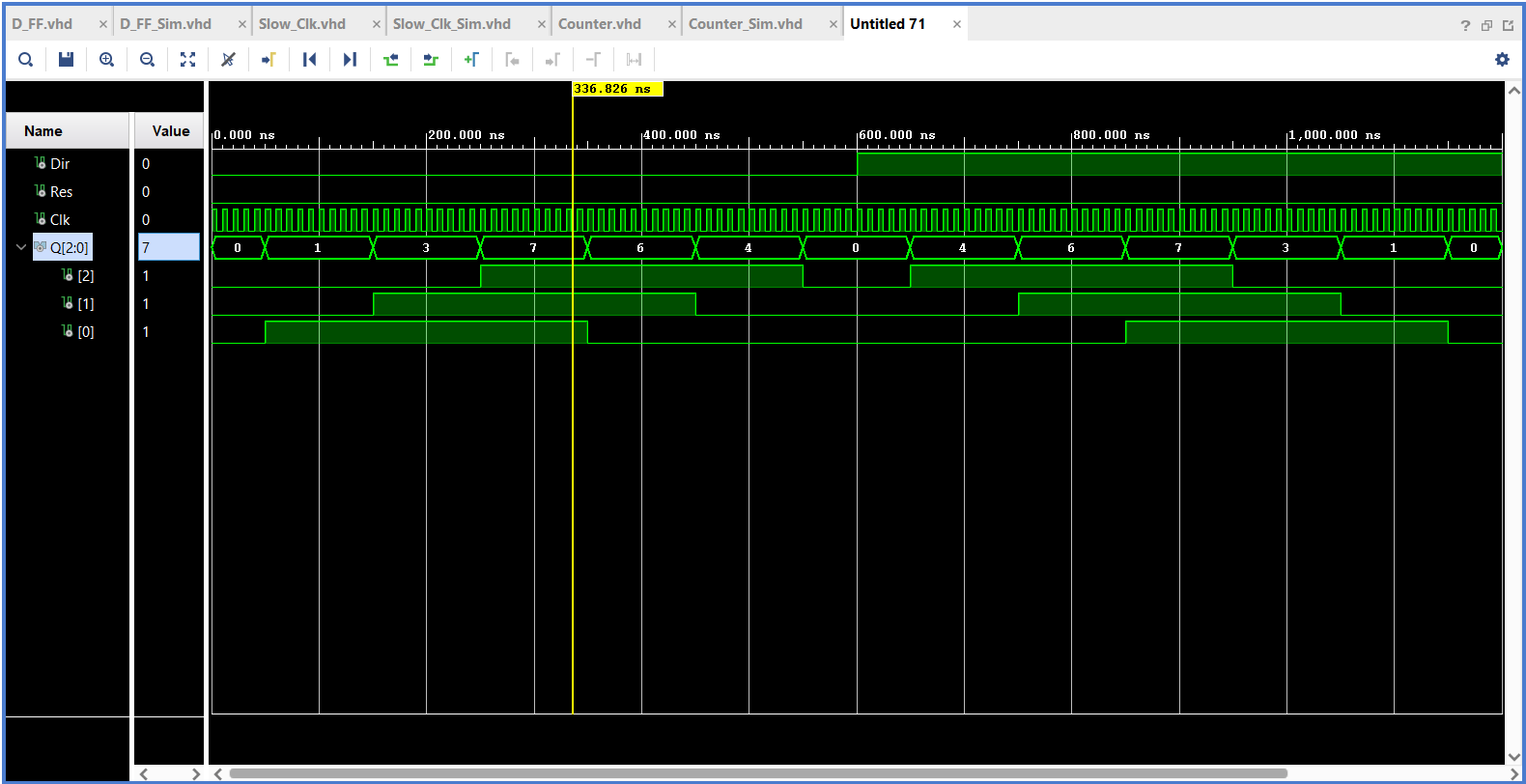
1. D Flip-Flop



1. Slowed-down Clock



1. Counter



**Conclusions:**

* I initialized some variables in order to get rid of undefined regions in the timing

diagrams.(Since all these elements are defined by their previous states, this is acceptable.)

* In ‘Slow\_Clk.vhd’, I did an experiment and found out that,

Clk\_out <= Clk\_status;

Clk\_status <= NOT Clk\_status;

&,

Clk\_out <= NOT Clk\_status;

Clk\_status <= NOT Clk\_status;

does the same thing. This is rather odd compared to the high-level programming

languages.